METHOD 2018.4

SCANNING ELECTRON MICROSCOPE (SEM) INSPECTIONS

1. PURPOSE. This method provides a means of judging the quality and acceptability of device interconnect metallization on non-planar oxide integrated circuit wafers or dice. SEM inspection is not required on planar oxide interconnect technology such as chemical mechanical polish (CMP) processes. It addresses the specific metallization defects that are batch process orientated and which can best be identified utilizing this method. Conversely, this method should not be used as a test method for workmanship and other type defects best identified using method 2010.

Samples submitted to SEM shall not be shipped as functional devices unless it has been shown that the device structure, in combination with the equipment operating conditions, is nondestructive.

1.1 Definitions.

1.1.1 Barrier adhesion metal. The lower layer of multi-layer metal system deposited to provide a sound mechanical bond to silicon/silicon oxide surfaces or to provide a diffusion barrier of a metal into an undesired area such as aluminum into a contact window.

1.1.2 Cross-sectional plane. An imaginary plane drawn perpendicular to current flow and which spans the entire width of the metallization stripe as illustrated in figure 2018-1. Metallization stripes over topographical variations (e.g., passivation steps, cross-overs, bird's head), which are nonperpendicular to current flow, are projected onto cross-sectional planes for purposes of calculating cross-sectional area reductions.

1.1.3 Destructive SEM. The use of specific equipment parameters and techniques that result in unacceptable levels of radiation damage or contamination of the inspected semiconductor structure.

1.1.4 Directional edge. A directional edge (see figure 2018-2) is typically the edge(s) of a rectangular contact window over which metallization may be deposited for the purpose of carrying current into, through, or out of the contact window for device operation. It should be noted that contact geometry, site of concern, or both may vary and if so, the directional edge concept should be modified accordingly.

1.1.5 General metallization (conductors). The metallization at all locations including metallization (stripes) in the actual contact window regions with the exception being at areas of topographical variation (e.g., passivation steps, bird's head, cross-overs).

1.1.6 Glassivation. Glassivation is the top layer(s) of transparent insulating material that covers the active circuit area (including metallization), except bonding pads and beam leads.

1.1.7 Interconnection. The metal deposited into a via to provide an electrical conduction path between isolated metal layers.

1.1.8 Major current-carrying directional edge. The directional edge(s) which is designed to provide a path for the flow of current into, through, or out of a contact window or other area(s) of concern (see figure 2018-2).

1.1.9 Multi-layer metallization (conductors). Two or more layers of metal used for electrical conduction that are not isolated from each other by a grown or deposited insulating material. The term "underlying metal" shall refer to any layer below the top layer of metal.

1.1.10 Multi-level metallization (conductors). A single layer or a multi-layer of metal shall represent a single level of metallization. A combination of such levels, isolated from each other by a grown or deposited layer of insulating material, shall comprise the multi-level metallization interconnection system. The use of vias to selectively connect portions of such level combinations through the isolation shall not effect this definition.

1.1.11 Nondestructive SEM. The use of specific equipment parameters and techniques that result in negligible radiation damage, contamination, or both of the inspected semiconductor structure (see 3.10 and 3.11).

1.1.12 Passivation. The silicon oxide, nitride or other insulating material that is grown or deposited on the die prior to metallization.

1.1.13 Passivation steps. The vertical or sloped surface resulting from topographical variations of the wafer surface (e.g., contact windows, diffusion cuts, vias, etc.).

1.1.14 Via. The opening in the insulating layer to provide a means for deposition of metal to interconnect layers of metal.

1.1.15 Wafer lot. A wafer lot consists of microcircuit wafers formed into a lot at the start of wafer fabrication for homogeneous processing as a group and assigned a unique identifier or code to provide traceability and maintain lot integrity throughout the fabrication process.

2. APPARATUS. The apparatus for this inspection shall be a scanning electron microscope (SEM) having resolution of 250Å or less as measured on the photograph at use conditions and a variable magnification of 1,000X to 20,000X or greater. The apparatus shall be such that the specimen can be tilted to a viewing angle (see figure 2018-3) between 0° and 85°, and can be rotated through 360°.

2.1 Calibration. The magnification shall be within ±10 percent of the nominal value when compared with National Institute of Standards and Technology standard 484 or an equivalent at the magnification(s) used for inspection. The resolution shall be 250Å or less as verified with National Institute of Standards and Technology standard SRM-2069 or equivalent. Magnification and resolution verification shall be performed on a frequency defined by the manufacturer based on statistical data for his SEM equipment.

2.2 Operating personnel. Personnel who perform SEM inspection shall have received adequate training in equipment operation and interpretation of the images and resulting photographs prior to attempting certification for metallization inspection. Procedures for certification of SEM operators for metallization inspection shall be documented and made available for review upon request to the qualifying activity, or when applicable, a designated representative of the acquiring activity. This shall include provisions for recertification procedures once a year as a minimum.

Operator certifications and recertifications shall be documented and made available for review upon request to the qualifying activity, or when applicable, a designated representative of the acquiring activity.

2.3 Procedures. There shall be written procedures for metallization inspection. These procedures shall be documented and made available for review upon request to the qualifying activity, or when applicable, a designated representative of the acquiring activity.

3. PROCEDURE.

3.1 Sample selection. Statistical sampling techniques are not practical here because of the large sample size that would be required. The wafer sampling requirements defined in table I, taken in conjunction with specific dice locations within the sampled wafers, minimize test sample size while maintaining confidence in test integrity. These dice are in typical or worst case positions for the metallization configuration.

Note: When die or packaged parts are to be evaluated for wafer lot acceptance and the requirements for wafer selection per Table I cannot be met, the following sample size shall be utilized:

a. If the die/packaged part is from a known homogeneous wafer lot (traceability specific to the wafer or wafer lot and objective evidence is available for verification), then the sample size shall be 8 devices randomly selected from the population.
b. If the die/packaged part is from a non-homogeneous wafer lot (traceability is unknown or no objective evidence is available for verification), then the sample size shall be 22 devices randomly selected from the population.

Die area submitted for SEM evaluation shall not have been or be located immediately adjacent to the wafers edge, and they shall be sufficiently free of smearing, so that the required inspection can be conducted in an area of undisturbed metallization. Acceptance of the interconnect metallization shall be based on examination of selected die area, using either a single wafer acceptance basis or a wafer lot acceptance basis.

Reference to die or dice within this test method implies the evaluation of a complete function or device. When approved by the qualifying activity, this requirement may be satisfied by the evaluation of a special SEM test vehicle existing within the scribe line (kerf), within each die, or within a special process drop in.

3.1.1 Sampling conditions. This sampling condition applies to devices which have glassivation over the metallization. Steps 1 and 2, which follow, both apply when acceptance is on a wafer lot acceptance basis. Step 2 applies only when acceptance is on a single wafer acceptance basis.

3.1.1.1 Step 1: Wafer selection. From each lot to be examined on a wafer lot acceptance basis, wafers shall be selected as defined by table I. If more than one wafer lot is processed through the metallization operation at one time, each wafer lot shall be grouped as defined by table I and a separate set of wafers shall be selected for each wafer lot being examined on a wafer lot acceptance basis.

3.1.1.2 Step 2: Dice selection. When a wafer is to be evaluated (for acceptance on a single wafer acceptance basis, or with one or more other wafers on a wafer lot acceptance basis), one of the following sampling conditions may be used at the manufacturer's option:

3.1.1.2.1 Sampling quadrants. Immediately following the dicing operation (e.g., scribe and break, saw, etch) and before relative die location on the wafer is lost, four dice shall be selected. The positions of these dice shall be approximately two-thirds of the radius (as measured from the center) of the wafer and approximately 90° apart. The glassivation shall then be removed from the dice using a suitable etchant process(es) (see 3.3) followed by SEM examination.

3.1.1.2.2 Sampling segment, prior to glassivation. This sampling condition may be used only if the subsequent wafer fabrication processing temperature is lower than 450°C (723K) and the width of the interconnect metallization is 3 microns or more. The use of this method with higher temperatures or smaller linewidths may be acceptable when correlation data, which shows there is no difference between this procedure and the normal etchback procedure, is submitted to and approved by the qualifying activity.

Two segments shall be separated from the opposite side of each wafer (i.e., subsequent to metallization and etching but prior to glassivation). These segments shall be detached along a chord approximately one-third of the wafer radius in from the edge of the wafer. One die approximately 1.5 cm from each end along the chord of each segment (i.e., four dice) shall be subjected to SEM examination.

3.1.1.2.3 Sampling segment, after glassivation. After completion of all processing steps and prior to dicing, two segments shall be separated from opposite sides of each wafer. These segments shall be detached along a chord approximately one-third of the wafer radius in from the edge of the wafer. One die approximately 1.5 cm from each end along the chord of each segment (i.e., four dice) shall be subjected to SEM examination after the glassivation has been removed using a suitable etchant process(es) (see 3.3).

3.1.1.2.4 Sampling whole wafers, prior to glassivation. This sampling condition may be used only if the subsequent wafer fabrication processing temperature is lower than 450°C (723K) and the width of the interconnect metallization is 3 microns or more. The use of this method with higher temperatures or smaller linewidths may be acceptable when correlation data, which shows there is no difference between this procedure and the normal etchback procedure, is submitted to and approved by the qualifying activity.

After completion of the metallization and etching steps and specimen preparation operation, if applicable (see 3.3), the complete wafer shall be placed into the SEM equipment and four die approximately two-thirds of the radius (as measured from the center) of the wafer and approximately 90° apart shall be inspected.

No die or contiguous die from the inspected wafer shall be shipped as a functional device unless it is shown that the examination is nondestructive (see 3.10 and 3.11).

3.1.1.2.5 Sampling whole wafers, after glassivation. This condition is destructive. The complete wafer shall be subjected to the specimen preparation operation, if applicable (see 3.3), and then placed into the SEM equipment. Four die approximately two-thirds of the radius (as measured from the center) of the wafer and approximately 90° apart shall be inspected.

TABLE I. Wafer sampling procedures for various metallization chamber configurations.

Metallization chamber configuration 1/ 2/	Number of wafer lots in chamber 3/	Required number of samples per wafer lot		Sampling plans per wafer lot
		Evaporation	Sputtering	
Projected plane view of the Wafer-holder is a circle. Wafer-holder is stationary or "wobbulates"	1 4/	5	2	Four from near the periphery of the wafer-holder and 90° apart. One from the center of holder. See figure 4.
	2	3, 4, or 5	2	See figure 4.
	3	3 or 4	2	See figure 4.
	4	3	2	See figure 4.
Wafer-holder is symmetrical (i.e., circular, square, etc.). Deposition source(s) is above or below the wafer-holder. Wafer-holder rotates about its center during deposition.	1, 2, 3, or 4 4/	2	2	For each wafer lot, one from the periphery of the wafer-holder, and one from close proximity to the center of rotation. See figure 4. 5/
Planetary system. One or more symmetrical wafer-holders (planets) rotate about their own axes while simultaneously revolving about the center of the chamber. Deposition source(s) is above or below the wafer-holders.	1, 2, 3, or 4 per planet 4/	2	2	For each wafer lot, one from near the periphery of a planet and one from near the center of the same planet. See figure 4. 6/
Continuous feed. Wafers are continuously inserted into deposition chamber through a separate pump down of an airlock (25 wafer nominal load)	1 1/	2	2	Two randomly selected wafers from each wafer lot.

1/ In this case, a wafer lot shall be defined as a batch of wafers which have received together those common processes which determine the slope and thickness of the passivation steps on these wafers.
2/ If a wafer-holder has only one circular row, or if only one row is used on a multi-rowed wafer-holder; the total number of specified sample wafers shall be taken from that row.
3/ If there is more than one wafer lot in a metallization chamber, each wafer lot shall be grouped approximately in a separate sector within the wafer-holder. A sector is an area of the circular wafer-holder bounded by two radii and the subtended arc; quadrants and semicircles are used as examples on figure 4.
4/ If the wafer lot size exceeds the loading capacity of the metallization system each processed sub-lot will be sampled as if it was a unique lot.
5/ When evaluation data shows that there is no relationship between SEM results and the physical location of the wafers during the metallization process. It shall be permissible to substitute two randomly selected wafers from each wafer lot. This analysis shall be repeated after each major equipment repair.
6/ Sample wafers need be selected from only one planet if all wafer lots contained in the chamber are included in that planet. Otherwise, sample wafers of the wafer lot(s) not included in that planet, shall be selected from another planet(s).

3.1.2 Sampling Destructive Physical Analysis (DPA) evaluation. Finished product, wafers, or die may be subjected to the test conditions and criteria defined within this test method for the purpose of a DPA evaluation.

3.2 Lot control during SEM examination. After dice selection for SEM examination, the manufacturer may elect either of two options:

3.2.1 Option 1. The manufacturer may continue normal processing of the lot with the risk of later recall and rejection of product if SEM inspection, when performed, shows defective metallization. If this option is elected, positive control and recall of processed material shall be demonstrated by the manufacturer by having adequate traceability documentation.

3.2.2 Option 2. Prior to any further processing, the manufacturer may store the dice or wafers in a suitable environment until SEM examination has been completed and approval for further processing has been granted.

3.3 Specimen preparation. When applicable, glassivation shall be removed from the dice using an etching process that does not damage the underlying metallization to be inspected (e.g., chemical or plasma etch). Specimens shall be mounted for examination in a manner appropriate to the apparatus used for examination. Suitable caution shall be exercised so as not to obscure features to be examined.

Specimens may be examined without any surface coating if adequate resolution and signal-to-noise levels are obtained. If the specimens need to be coated, they shall be coated with no more than 100Å of a thin vapor-deposited or sputtered film of a suitable conductive material (e.g., Au). The coating deposition process shall be controlled such that no artifacts are introduced by the coating.

3.4 Specimen examination, general requirements. The general requirements for SEM examination of general metallization and passivation step coverage are specified below in terms of directional edge, magnification, viewing angle, and viewing direction.

3.4.1 Directional edge. All four directional edges of every type of passivation step (contact window or other type of passivation step) shall be examined on each specimen (see table II).

3.4.2 Magnification. The magnification used for examination of general metallization and passivation steps shall be within the range defined by table II.

3.4.3 Viewing angle. Specimens shall be viewed at whatever angle is appropriate to accurately assess the quality of the metallization. Contact windows, metal thickness, lack of adhesion, and etching defects are typically viewed at the angles of 0° to 85° (see figure 2018-3).

3.4.4 Viewing direction. Specimens shall be viewed in an appropriate direction to accurately assess the quality of the metallization. This inspection shall include examination of metallization at the edges of contact windows and other types of passivation steps (see 3.4) in any direction that provides clear views of each edge and that best displays any defects at the passivation step. This may mean that the viewing angle is perpendicular to an edge, or in parallel with an edge, or at some oblique angle to an edge, whichever best resolves any question of defects at the passivation step (see figure 2018-5).

3.5 Specimen examination detail requirements. Examination shall be as specified herein and summarized in table II. The specimen examination shall be documented in accordance with 3.8.

3.5.1 General metallization. At low magnification, inspect at least 25 percent or 10,000 square mils, whichever is less, of the general metallization on each die for defects such as lifting, peeling, blistering, and voiding. Inspection shall be performed for each layer of each level of metallization.

3.5.1.1 Multi-layer and multi-level metal interconnection systems. Each layer of each metallization level that is deposited shall be examined. The current- carrying layer(s) shall be examined with the SEM after removal of the glassivation layer (if applicable) with a suitable etchant (see 3.3).

3.5.1.2 Barrier/adhesion layers. The examination of barrier/adhesion layers designed to conduct less than 10% of the total current is not required as this is considered a non-conduction layer.

3.5.1.2.1 Barrier/adhesion layer as a conductor. The barrier/adhesion layer shall be considered as a conductor (considering the layer thickness and relative conductivity) provided that the following conditions are satisfied: At least ten percent of the current is designed to be carried by this layer; and this layer is used in the current density calculations. When this occurs the barrier/ adhesion layer and/or the principal conducting layer shall satisfy all of the step coverage requirements collectively as baselined by the manufacturer. Specimen examination shall be in accordance with 3.5 and the accept/reject criteria as defined in 3.7.1. The barrier/adhesion layer(s) shall be examined using either the SEM or optical microscope. The following methods may be used to examine these barrier/adhesion layers:

3.5.1.2.1.1 The Etchback procedure. This involves the stripping of each successive unique layer of metal by selective etching, with suitable etchants, layer by layer, to enable the examination of each layer. Typically, each successive layer of metal will be stripped in sequence to expose the next underlying layer for examination. Successive layer removal on a single die area may be impractical. In this case the wafer area or additional die (dice) immediately adjacent on the slice to the original die area shall be stripped to meet the requirement that all unique layers shall be exposed and examined.

3.5.1.2.1.2 In-line procedure. The wafer(s) shall be inspected for the defined accept/reject criteria immediately after being processed through each unique deposition and corresponding etching operation.

3.5.2 Passivation steps. Inspect the metallization at all types of passivation steps in accordance with the requirements of 3.5.1.1 and table II.

TABLE II. Examination procedure for specimens.

Device type	Area of examination	Examination	Minimum-maximum magnification	Photographic documentation 1/
Integrated circuit devices	Passivation steps (contact windows and other types of passivation steps) 2/	At least one of each type of passivation step present	5,000X to 50,000X	Two of the worst case passivation steps
	General metallization 2/	25 percent	1,000X to 6,000X	Worst case general metallization

1/ See 3.8 (an additional photograph may be required).
2/ See 3.7 for accept/reject criteria.

3.6 Acceptance requirements.

3.6.1 Single wafer acceptance basis. The metallization on a single wafer shall be judged acceptable only if all the sampled areas or dice from that wafer are acceptable.

3.6.2 Wafer lot acceptance basis. An entire wafer lot shall be judged acceptable only when all the sampled areas or dice from all sample wafers are acceptable. If a wafer lot is rejected in accordance with this paragraph each wafer from that wafer lot may be individually examined; acceptance shall then be in accordance with 3.6.1.

3.7 Accept/reject criteria. Rejection of dice shall be based on batch process defects and not random defects such as scratches, smeared metallization, tooling marks, etc. In the event that the presence of such random defects obscures the detailed features being examined, an additional adjacent sample shall be inspected. Illustrations of typical defects are shown in figures 2018-6 through 2018-22.

3.7.1 General metallization. Any evidence of poor metallization adhesion shall be unacceptable. Any defects (see figure 2018-18 and 2018-20), such as voids, cracks, separations, depressions, notches, or tunnels, which singly or in combination reduce the cross-sectional area of the general metallization stripe by more than 50 percent shall be unacceptable. Two specific cases of general metallization are specified below:

3.7.1.1 Conductor stripes. In the examination of the other metal layers for the specific case of conductor stripes (exclusive of the contact window area), a defect consuming 100 percent of the thickness of the barrier/adhesion stripe shall be acceptable provided that the defect does not extend more than 50 percent across the width of the metallization stripe (see figure 2018-22).

3.7.1.2 Barrier layers in contact window areas. No defects of any kind in a barrier layer which would bring the overlying metal layer in contact with the semiconductor material surface shall be permitted.

3.7.1.3 Overlying adhesion layers. For the metal layer(s) above the principal conducting layer, a defect consuming 100 percent of the thickness of the adhesion stripe shall be acceptable provided that the defect does not extend more than 50 percent across the width of the metallization stripe.

3.7.2 Passivation steps. Metallization over a passivation step shall be unacceptable if any combination of defects (see figure 2018-23) or thinning of the metal reduces the cross-sectional area of the metallization stripe along any cross-sectional plane in a major current-carrying direction to less than 50 percent of the cross-sectional area of the stripe. A minimum of 20 percent total metallization coverage (barrier metal inclusive, see figure 2018-24) in the primary current carrying direction will be allowed for metallization over a passivation step when the structure involved is a circular or multisided via or contact structure and there is sufficient wrap-around metal (>10 percent of incoming metal line width) to allow for current flow to all sides of the via or contact. The metallization must meet the current density requirements of MIL-PRF-38535. In cases where an absence of visible edge or a smooth transition or taper clearly reveals effective coverage, a cross-section will be performed to verify metal coverage.

3.7.2.1 Nonrejectable cross-sectional area. In the event that the metallization cross-sectional area at a particular directional edge profile is less than as allowed in 3.7.2. This shall not be cause for rejection if the following two conditions occur:

3.7.2.1.1 Condition 1. It is determined that the directional edge profile from which metal is absent does not occur in the major current-carrying directional edge. Such determination shall be made either by scanning all passivation steps of this type on the remainder of the die, or by the examination of a topographical map supplied by the manufacturer which shows the metal interconnect pattern.

3.7.2.1.2 Condition 2. Acceptance shall be on a single wafer basis only.

3.7.2.2 Nonrejectable, noncovered directional edge. For passivation steps to be acceptable, all directional edges shall be covered with metallization and be acceptable to the requirements of 3.7.2.1, unless by design. In the event that a directional edge profile of a particular type of passivation step is not covered with metallization, this shall not be cause for rejection if the following two conditions occur:

3.7.2.2.1 Condition 1. It is determined that the directional edge profile from which metal is absent does not occur in the major current-carrying directional edge. Such determination shall be made either by scanning all passivation steps of this type on the remainder of the die, or by the examination of a topographical map supplied by the manufacturer which shows the metal interconnect pattern.

3.7.2.2.2 Condition 2. None of the other specimens from the sampled wafers representing the lot exhibit a directional edge profile from which metal is absent in the major current-carrying directional edge.

NOTE: If both 3.7.2.2.1 and 3.7.2.2.2 are satisfied, a wafer lot acceptance basis shall be used. However, if only 3.7.2.2.1 is satisfied, a single wafer acceptance basis shall be used.

3.7.3 Verification of potential rejects. At the option of the manufacturer, it shall be permissible to subject the specimen, or an adjacent sample that exhibits the same reject mode, to a verification test. Given below are some examples of suitable verification tests:

3.7.3.1 Cross-sectioning. A passivated sample shall be cleaved or lapped down to bisect the area of concern. The sample may then be subjected to an etchant that will remove the interconnecting metallization at the inspection surface (i.e., approximately perpendicular to the die surface). Specimens may be examined without any special surface coating if surface charging is not a significant problem and adequate resolution and signal-to-noise levels are obtained. If the specimens are coated, they shall be coated with a thin vapor-deposited or sputtered film of a suitable conductive material (i.e., 100Å gold). The coating deposition processes shall be controlled such that no artifacts are introduced by the coating. The sample shall be prepared (see 3.3) and examined in the SEM for interconnect metallization thickness or percentage coverage at the passivation step, or any other relevant parameter. Note: This cross-sectioning technique is not conclusive for hairline microcracks as they are not adequately filled by the passivation material.

3.7.3.1.1 Dimensional errors. Care must be taken to ensure that the cross-section is close to the center of a contact in order to avoid dimensional errors due to the rounding of the contact corners.

3.7.3.2 Surface etchback. The unpassivated sample surface is subjected to a chemical etch which removes the interconnection metallization from the surface of the die at a known controlled rate. The etching is stopped when the required metal thickness has been removed. The sample is then prepared (see 3.3) and examined within the SEM for residual metal at the passivation step/contact window interface. Photographic evidence shall then be taken of the sample(s) to support the acceptance or rejection of the material.

3.7.3.3 Topographical integration. A graphical representation of the worst case cross-sectional area is drawn to scale on appropriate graph paper from comprehensive photographs taken eucentrically about the directional edge. The cross-sectional area is then graphically integrated. This technique is useful for evaluating metallization with irregular surface topography.

3.8 Specimen documentation requirements. A minimum of three photographs for each layer of each level of metallization inspected per lot shall be taken and retained for a minimum of five years after performance of the inspection. Two photographs shall be of worst case passivation steps and the third photograph of worst case general metallization. If any photograph shows an apparent defect within the field of view, another photograph shall be taken to certify the extent of the apparent defect (see table II).

NOTE: Alternate methods of image storage (e.g., video disk or video tape) shall be acceptable with the prior approval of the qualifying activity.

3.8.1 Required information. The following information shall be traceable to each photograph:

a. Date of SEM photograph.

b. Device or circuit identification (type or part number).

c. Area of photographic documentation.

d. Electron beam accelerating voltage.

e. Magnification.

f. Manufacturer.

g. Manufacturer's lot identification number.

h. Record of calculated/measured percentage step coverage.

i. SEM operator or inspector's identification.

j. Viewing angle.

3.9 Disposition of inspected specimens. SEM samples and contiguous die shall not be shipped as functional devices unless nondestructive SEM conditions and requirements are met (see 3.10). In order to be considered nondestructive, suitable life-test data (see 3.11) shall be submitted for approval to the qualifying activity to substantiate the nondestructive aspects of the test (e.g., radiation hardness degradation-RHD). Additionally, all of the conditions in 3.10 and 3.11 must be satisfied.

3.10 Nondestructive SEM conditions. For nondestructive SEM, the following conditions shall apply:

3.10.1 Equipment conditions.

a. The accelerating voltage shall be within the 0.5 kV to 2.0 kV range.

b. The absorbed specimen current (as measured with a Faraday cup) shall be less than 500 pA.

c. Total scan time for each test site on the wafer shall not exceed ten minutes.

d. Resolution for metal inspection shall be in accordance with 2 above at the accelerating voltage of 3.10.1a. When used for other in-line nondestructive SEM evaluations (e.g., photoresist, critical dimension (cd) inspection, etc.) the resolution shall be sufficient to clearly verify the measurement.

3.10.2 Wafer conditions.

a. The wafer lot shall satisfy the thermal stability criteria defined within MIL-STD-883, method 5007, table I.

b. Weekly monitoring of particle counts shall be conducted in the SEM inspection area. The particle count limits shall be less than or equivalent to the specified wafer fab limits.

c. The wafer shall be clean and free of any surface coating.

3.11 Required data for nondestructive SEM validation. Data demonstrating that the method is nondestructive as defined in A.4.3.2.2 of Appendix A of MIL-PRF-38535 shall be submitted to the qualifying activity following the procedure detailed in 3.11.1 through 3.11.3.

3.11.1 Sample conditioning. Expose a sufficient number of devices to the following conditions to yield a quantity of life test samples that meet a quantity (accept number) of 45(0) for each validation sample:

a. Sample A: Expose at the worst case SEM operating conditions (i.e., accelerating voltage, absorbed specimen current and tilt) and normal SEM metallization inspection procedure for a duration of 10 ± 1 minutes.

b. Sample B: Expose at the worst case SEM operating conditions and normal SEM metallization inspection procedure for an increased duration of 30 ± 3 minutes.

c. Sample C: (Optional at the discretion of the manufacturer.) Control group without any SEM exposure.

3.11.2 Procedure. Process test groups through all normal screening steps to complete post burn-in electricals, serialize test samples, and complete 3.11.2a through 3.11.2d.

a. Data log variables on all 25°C dc parameters and record attributes data for all other group A electrical test parameters, conditions and limits specified in the device specification or drawing (i.e., complete group A, not only specified life test endpoints).

b. Place test samples, including the control group if applicable, on life test in accordance with method 1005 at 125°C minimum for 1630 hours or equivalent (130°C for 1,135 hours, 135°C for 800 hours, 140°C for 565 hours, 145°C for 405 hours, 150°C for 295 hours, 155°C for 215 hours, 160°C for 155 hours, 165°C for 115 hours, 170°C for 85 hours, 175°C for 65 hours) with cooldown under bias using test condition C.

c. Repeat 3.11.2a for post life test endpoints.

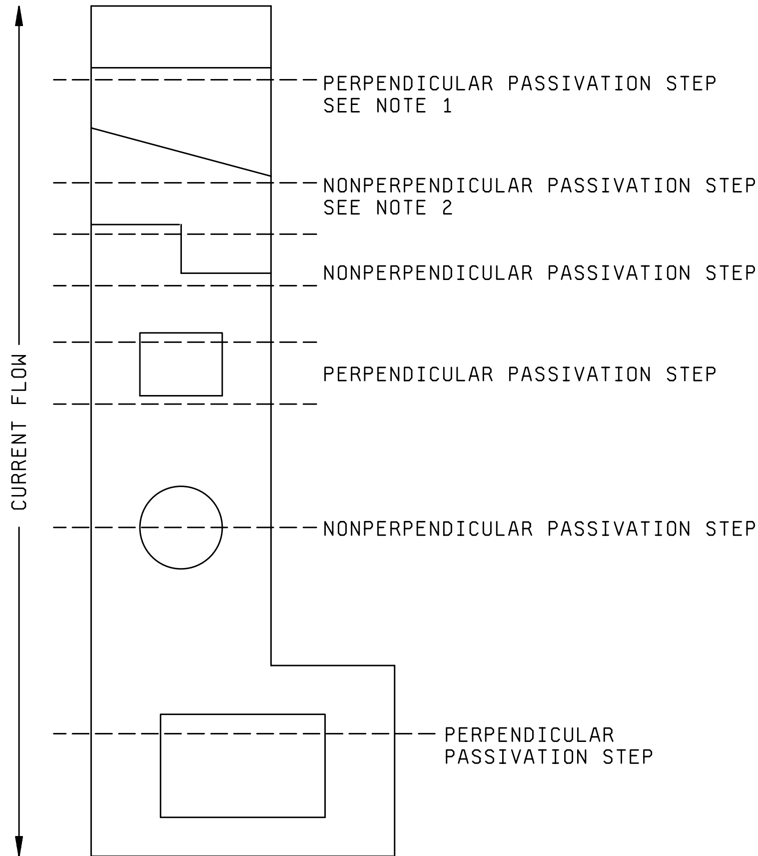
d. Provide qualifying activity with one set of test results for each sample in terms of variables and attributes data on pre and post life test endpoints plus analysis of mean and standard deviation of variables data and indication of any devices which failed any group A test parameters.

3.11.3 Criteria for validating SEM as nondestructive. If sample A passes single duration and sample B passes triple duration SEM exposure and life test without failing any device specification or drawing parameters, conditions and limits (or delta parameter requirements when they are specified), the SEM procedure shall be validated as nondestructive for the process flow represented by the sample devices and for other devices from the same process flow. With the approval of the qualifying activity, this SEM nondestructive qualification may be performed on appropriate process monitor structures or standard evaluation circuits (SEC's) which represent the process flow.

4. SUMMARY. The following details may be specified in the applicable acquisition document:

4.1 Detail 1. Single wafer acceptance basis when required by the acquiring activity.

4.2 Detail 2. Requirements for photographic documentation (number and kind) if other than as specified in 3.8.



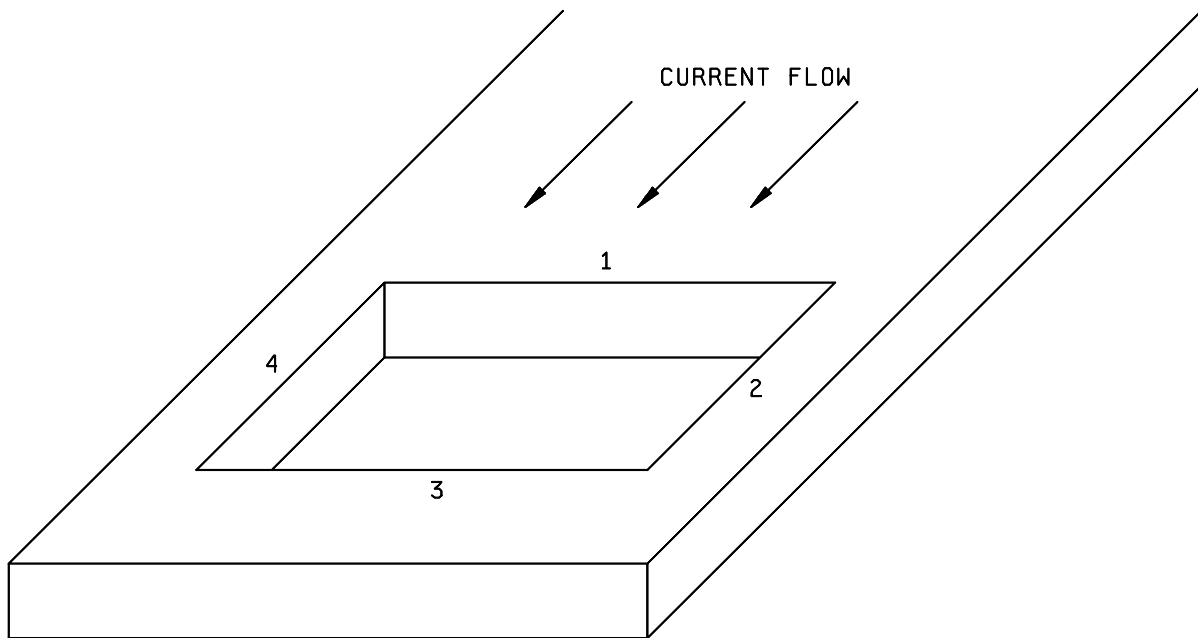
NOTES:

1. Cross-sectional planes are denoted by dashed lines.
2. All passivation steps nonperpendicular to current flow must be projected onto cross-sectional planes perpendicular to current flow for purpose of cross-sectional area calculations.
3. The purpose of this cross-sectional plane illustration is two-fold:

   To provide a consistent and convenient means to facilitate the calculation of the appropriate cross-sectional area.

   To insure that the cross-sectional area of the metallization in a major current carrying direction is reduced to no more than 50 percent (30 percent when appropriate) for the topographical variation under consideration.

FIGURE 2018-1. Cross-sectional planes at various passivation steps.



NOTES:
1. 1, 2, 3, and 4 are directional edges.
2. 1 is a major current carrying edge.

FIGURE 2018-2. Directional edge.

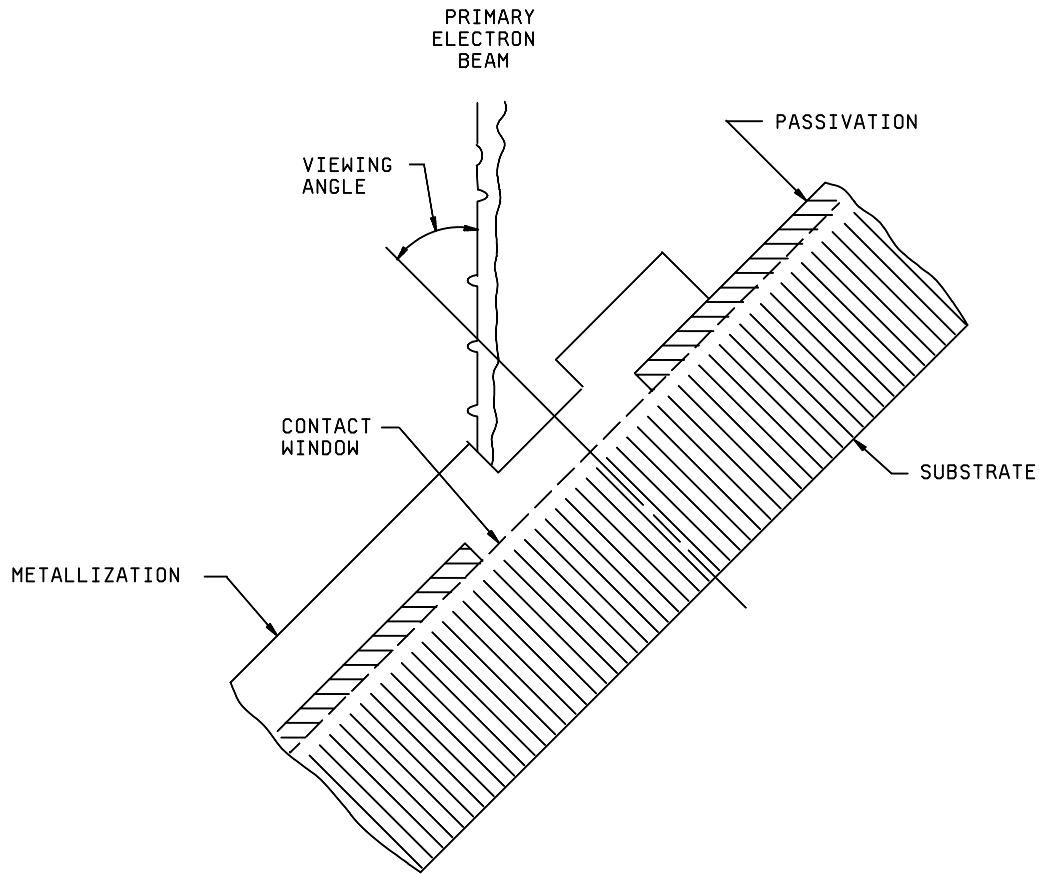
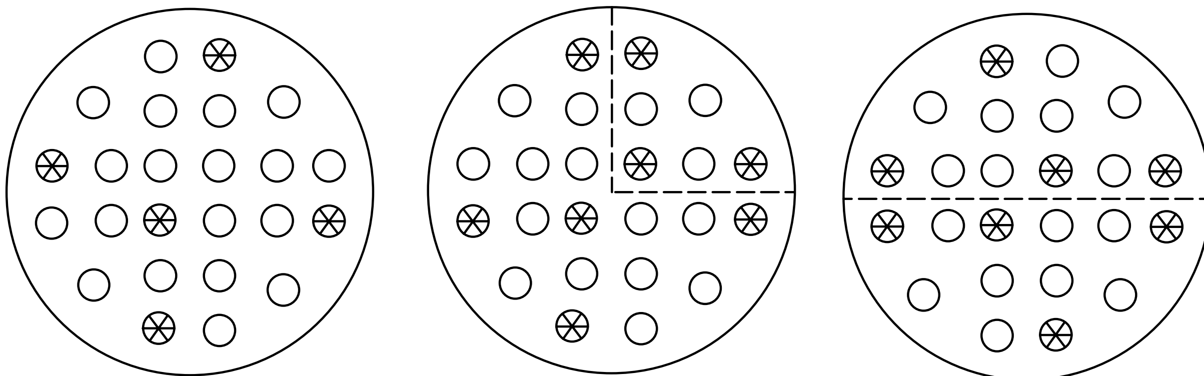
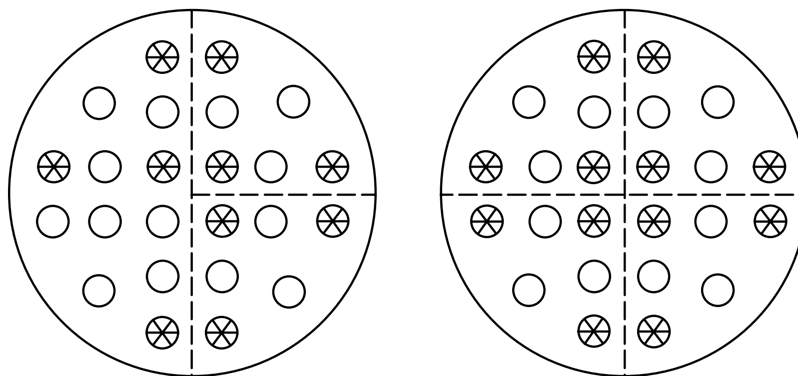


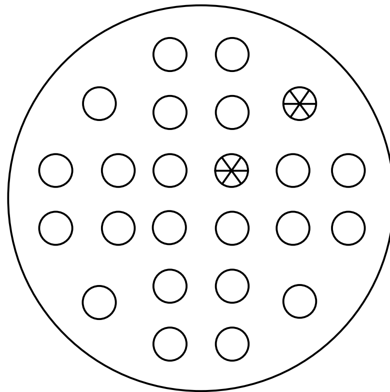
FIGURE 2018-3. Viewing angle.



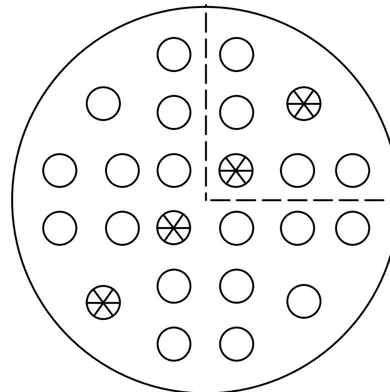


STATIONARY (EVAPORATION) WAFER-HOLDER SYSTEM

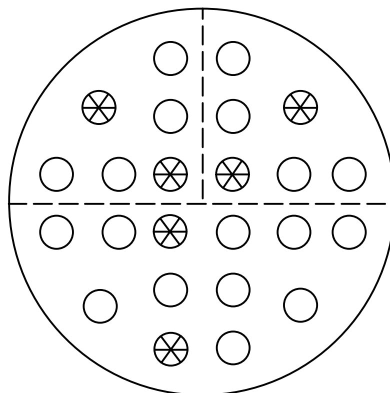
FIGURE 2018-4. Wafer sampling procedures (see table I).



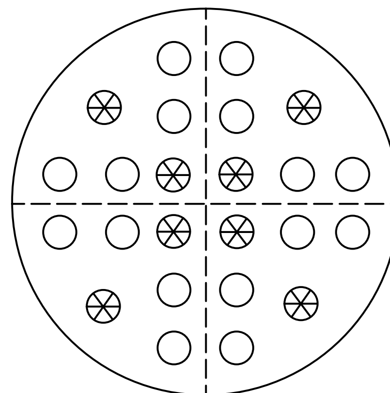
One wafer lot



Two wafer lots



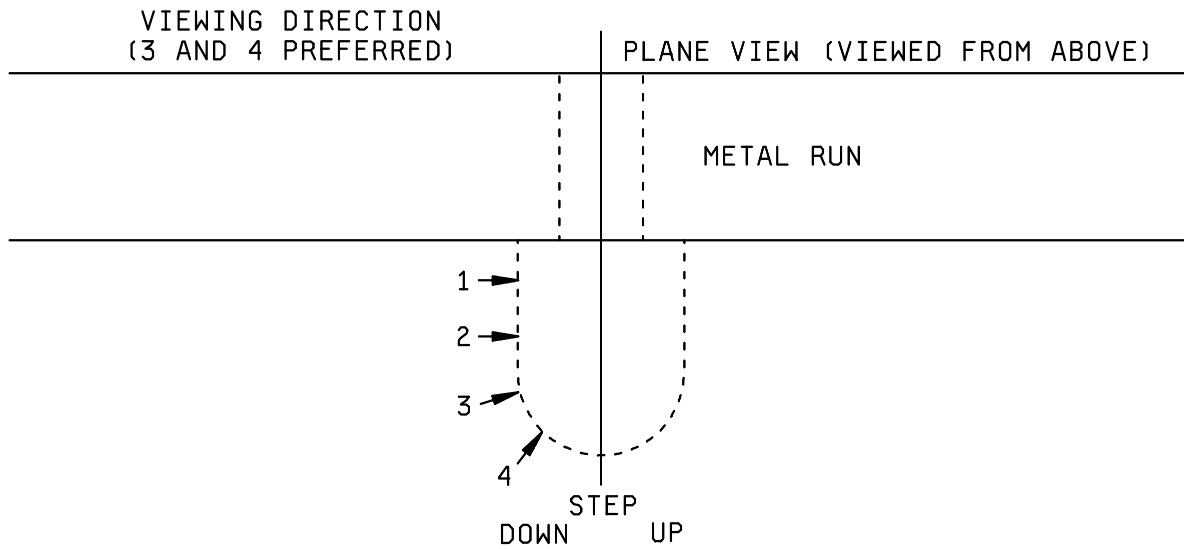
Three wafer lots



Four wafer lots

ROTATING STATIONARY (SPUTTERING) PLANETARY OR CONTINUOUS FEED WAFER-HOLDER SYSTEM

FIGURE 2018-4. Wafer sampling procedures (see table I) - Continued.



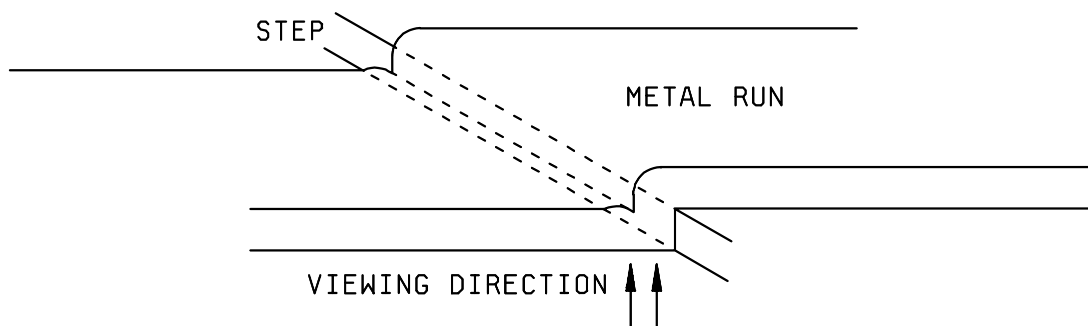


FIGURE 2018-5. Viewing direction.

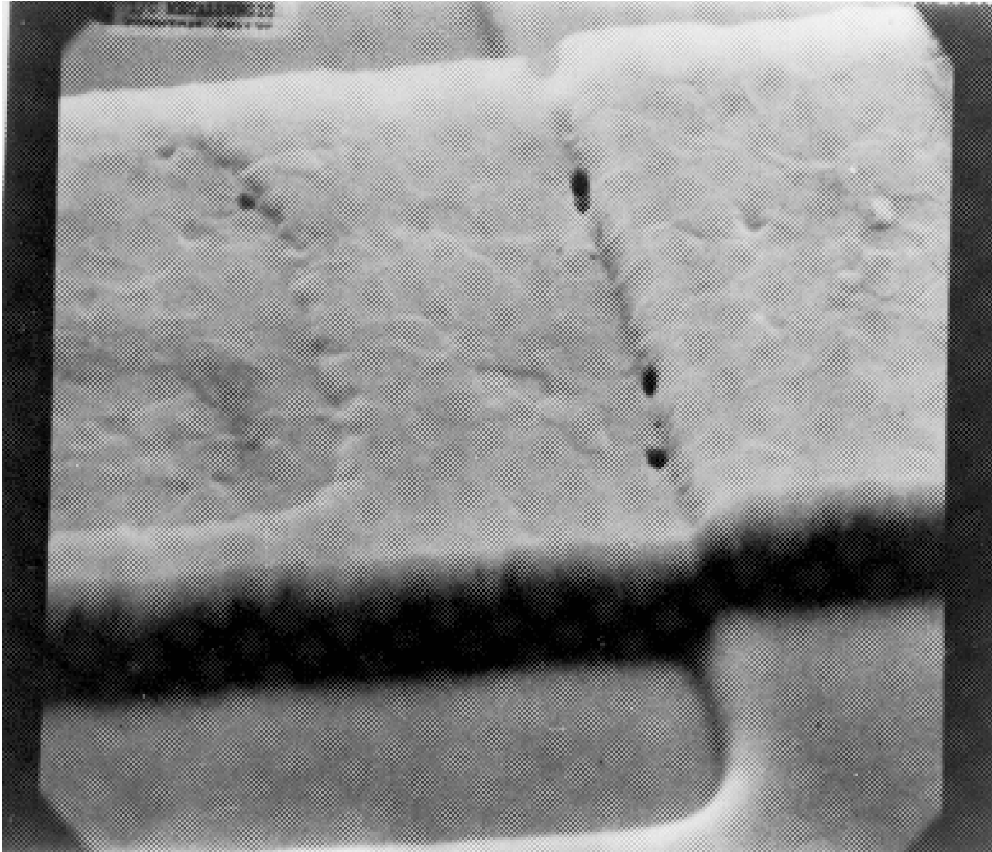


FIGURE 2018-6. (3,400X).
Voiding at passivation step (accept).

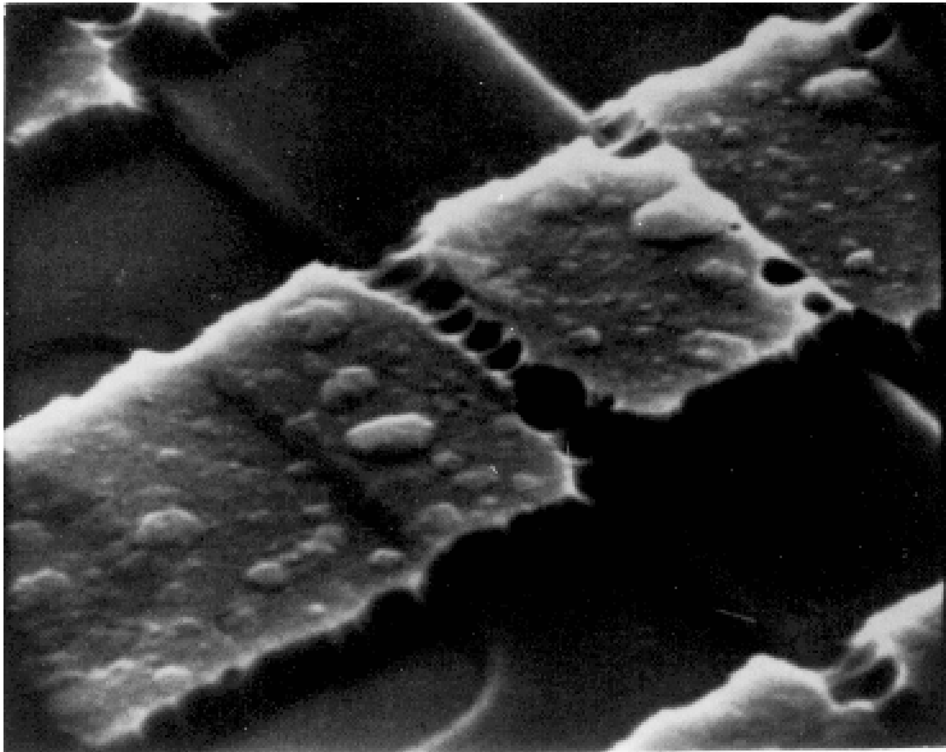


FIGURE 2018-7. 5,000X.
Voiding at passivation step (reject).

NOTE: Tunnel does not extend to surface
of metal; does not reduce cross-sectional
area more than 50 percent.

FIGURE 2018-8. (10,000X).
Tunnel/cave at passivation step (accept).

FIGURE 2018-9. 5,000X.
Tunnel/cave at passivation step (reject).

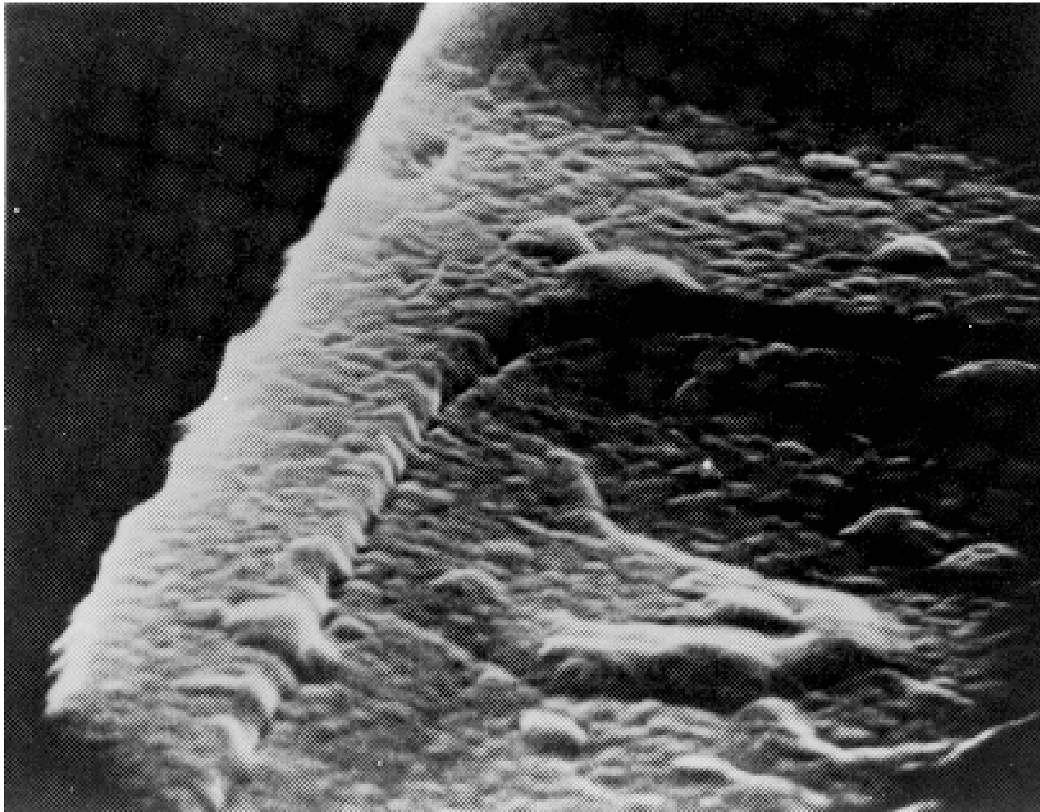


FIGURE 2018-10. (10,000X).
Separation of metallization at
passivation step (base contact) (accept).

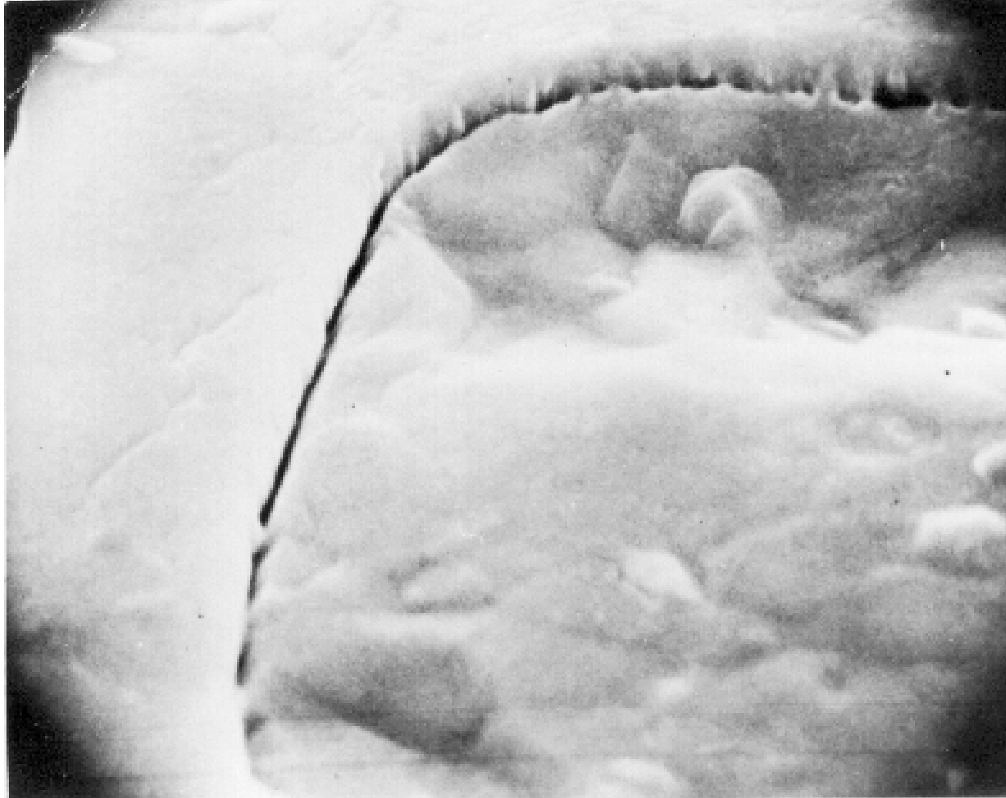


FIGURE 2018-11. 7,000X.
Separation of metallization at
passivation step (base contact) (reject).

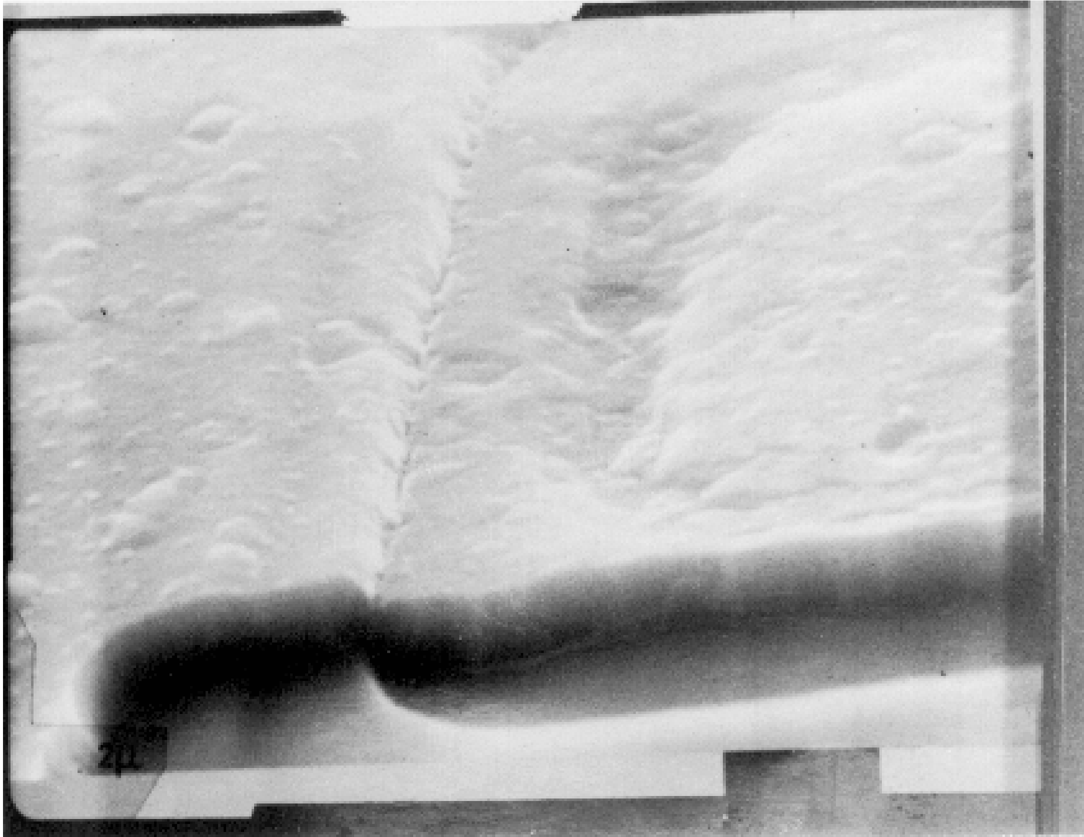


FIGURE 2018-12. (6,000X).
Crack-like defect at passivation step (accept).

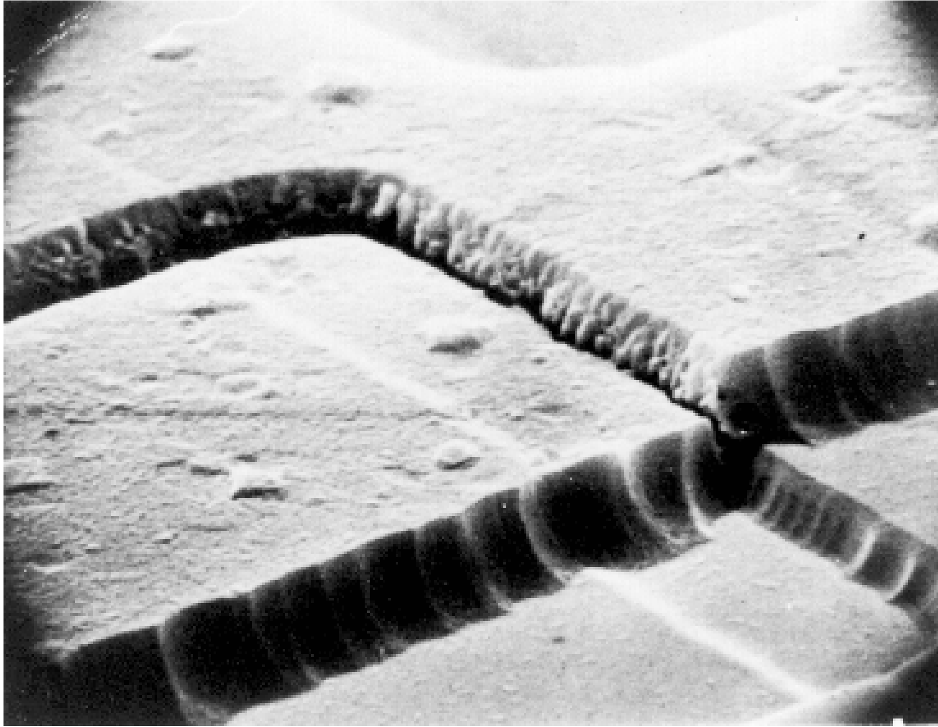


FIGURE 2018-13. 6,000X.
Crack-like defect at passivation step (reject).

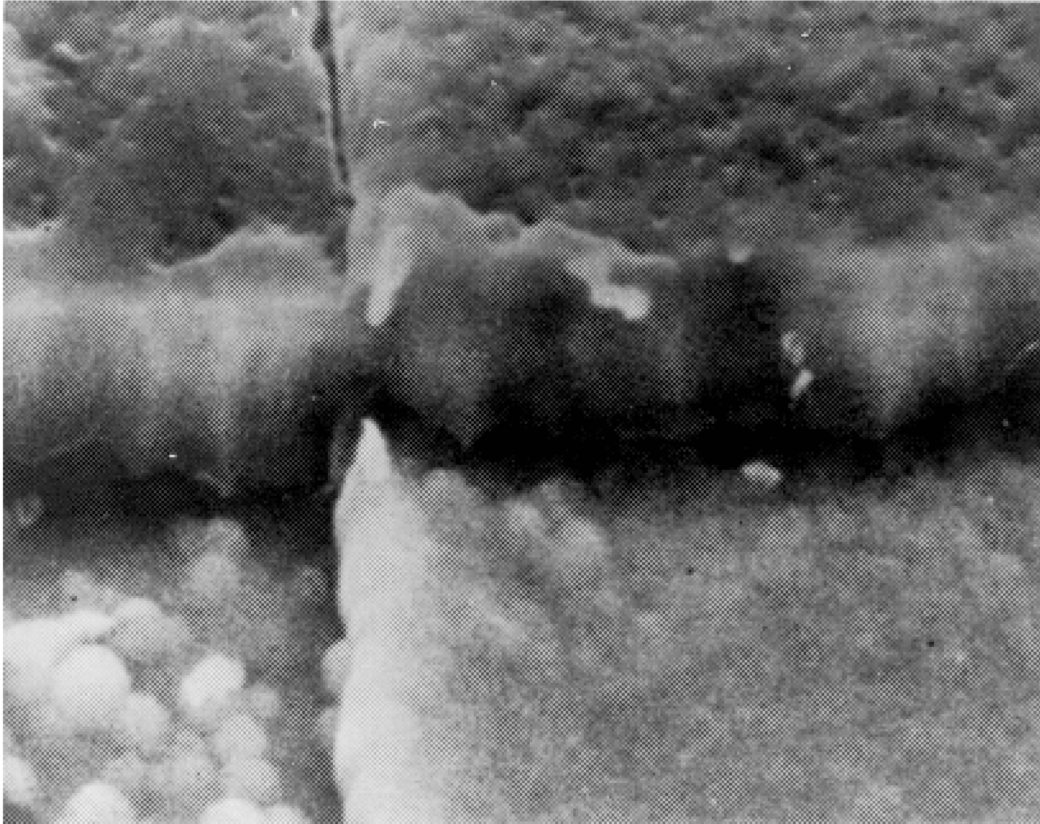


FIGURE 2018-14. (7,200X).
Thinning at passivation step with more than 50 percent of cross-sectional area remaining at step (multi-level metal) (accept).

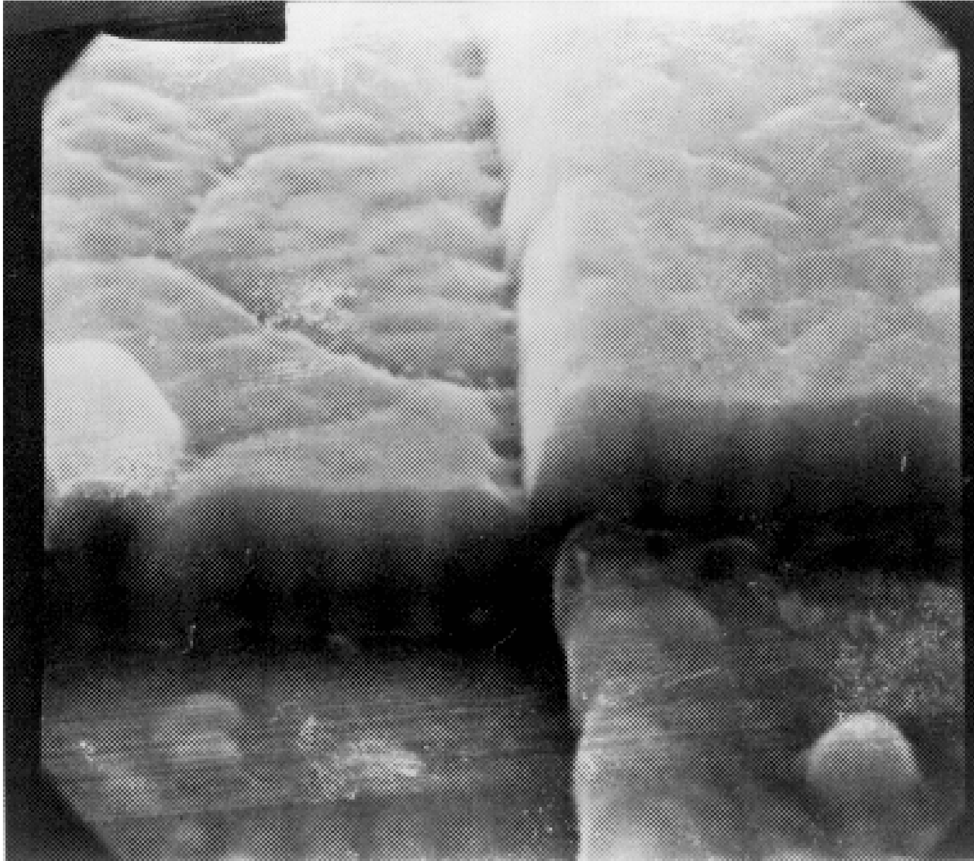


FIGURE 2018-15. 7,200X.
Thinning at passivation step with less than 50 percent of cross-sectional area remaining at step (multi-level metal) (reject).

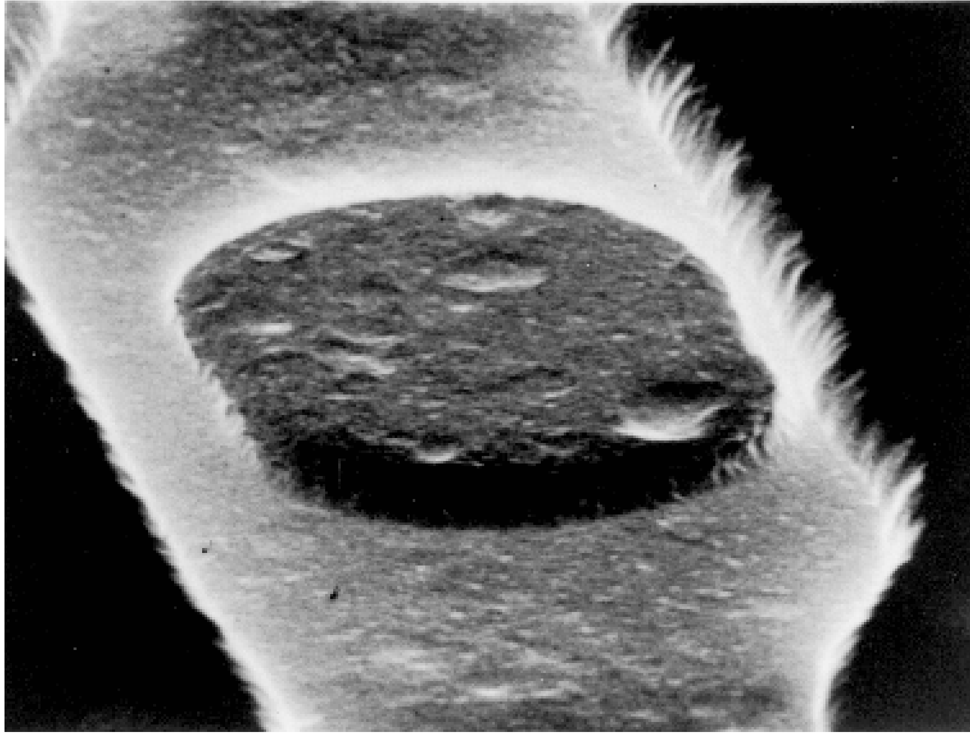


FIGURE 2018-16. (6,000X).
Steep passivation step (MOS) (accept).

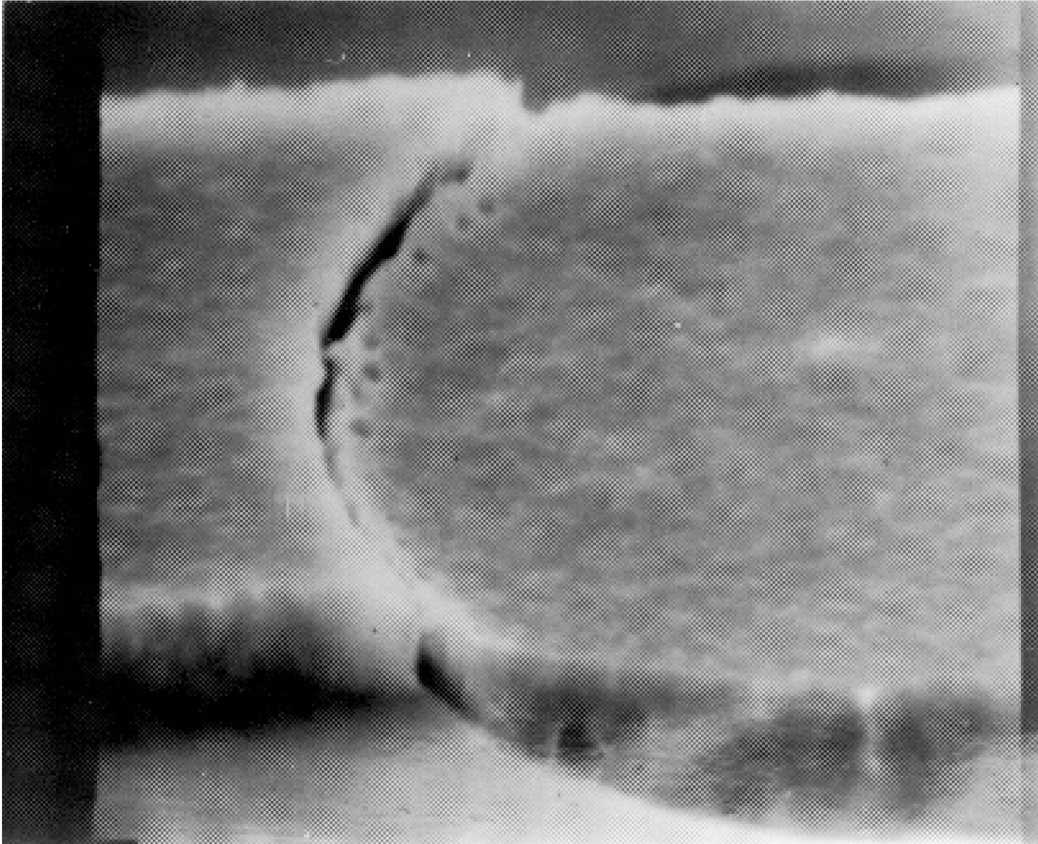


FIGURE 2018-17. 9,500X.
Steep passivation step (MOS) (reject).

FIGURE 2018-18. (5,000X).
Peeling or lifting general metallization
in contact window area (reject).

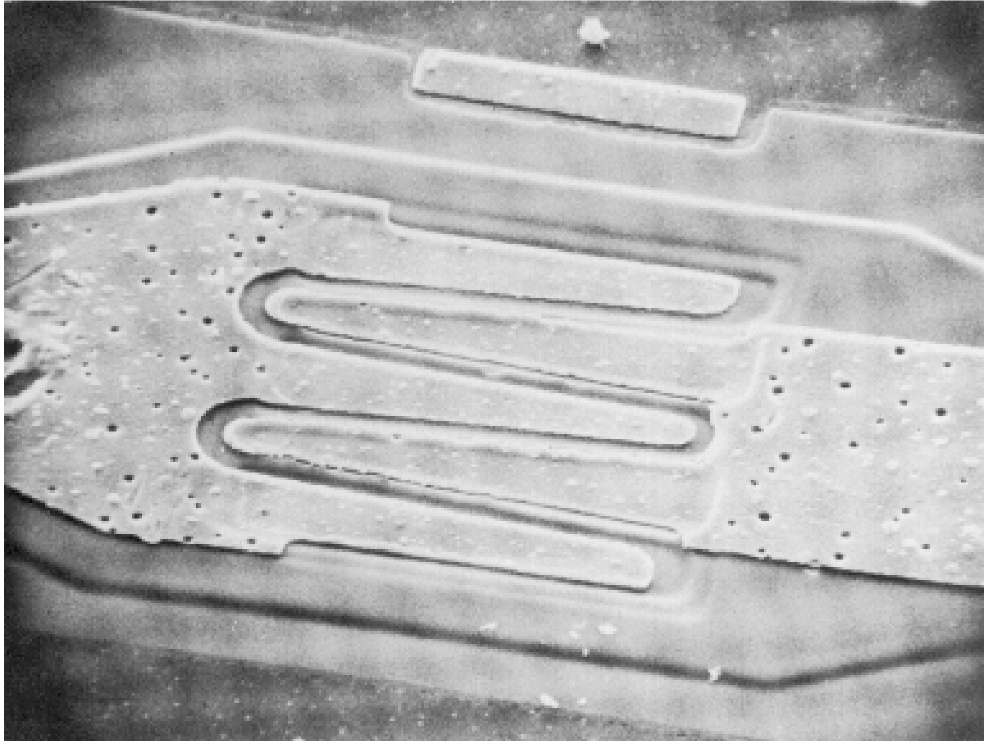


FIGURE 2018-19. 10,000X.
General metallization voids (accept).

FIGURE 2018-20. (5,000X).
General metallization voids (reject).

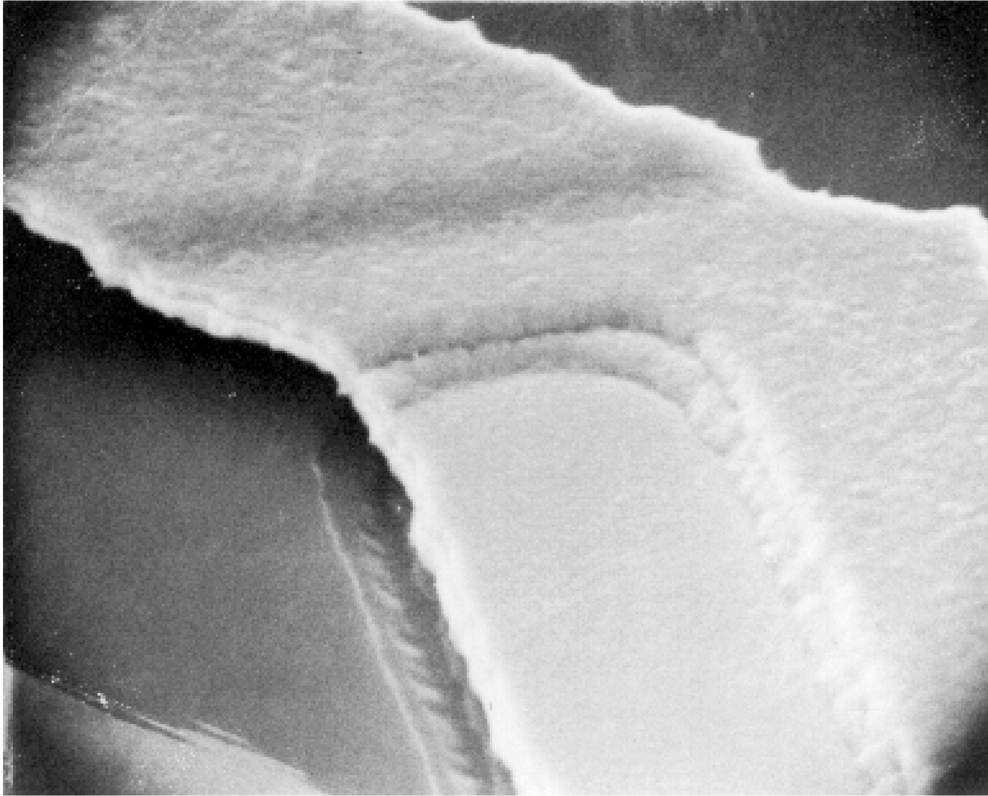


FIGURE 2018-21. 5,000X.
Etch-back/undercut type of notch at
passivation step (multi-layered metal) (accept).

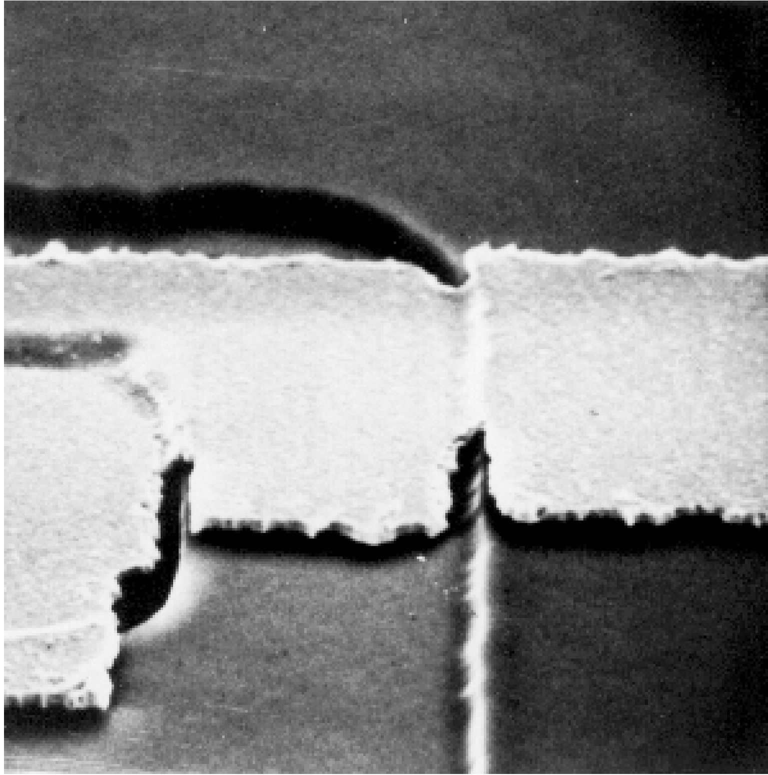
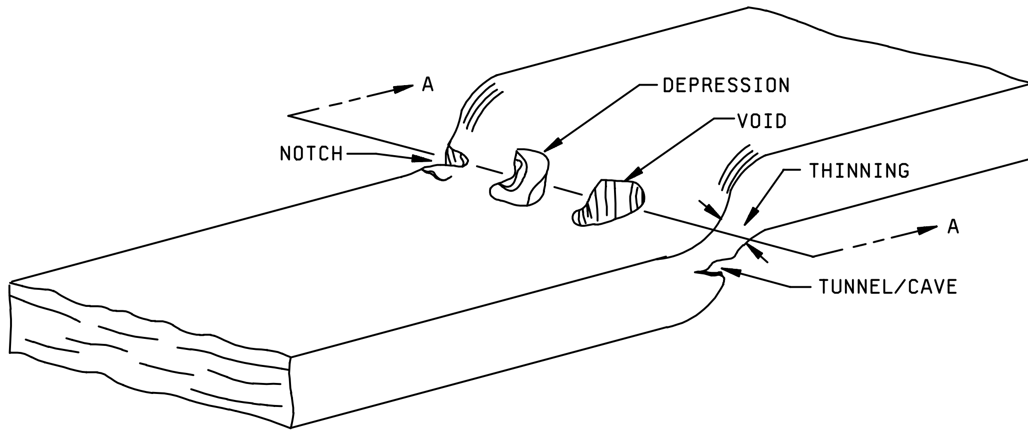
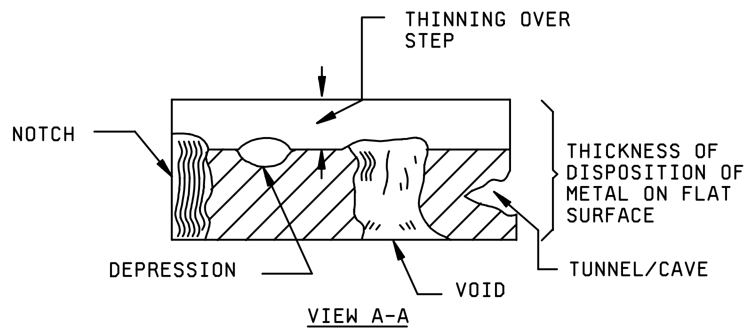


FIGURE 2018-22. (5,000X). Barrier or adhesion layer etch-back/undercut type of notch at passivation step (multi-layered metal) (accept).



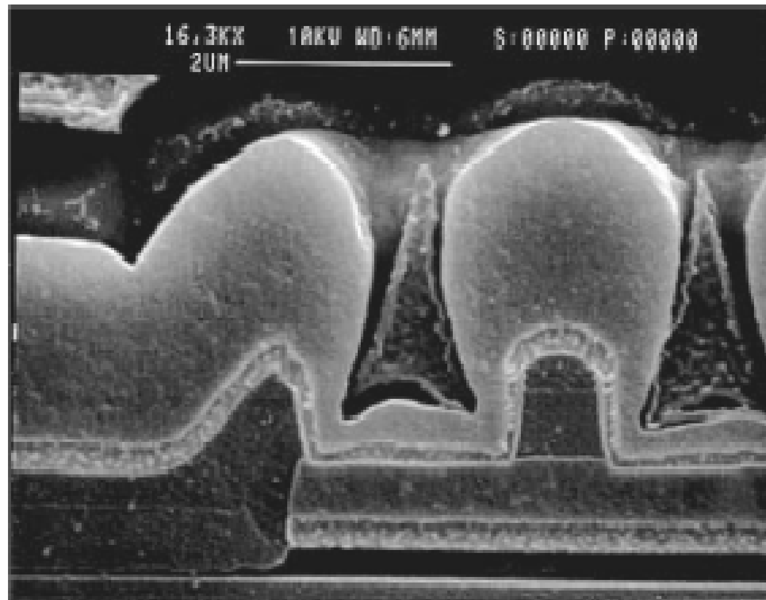
METALLIZATION AT PASSIVATION
STEP SHOWING TYPICAL DEFECTS



VIEW A-A

CROSS-SECTION AREA (ENLARGED) OF METALLIZATION
AT PASSIVE STEP SHOWN ABOVE

FIGURE 2018-23. Concept of reduction of cross-sectional area of metallization as accept/reject criteria (any combination of defects and thinning over a step which reduces the cross-sectional area of the metal to less than the percentage defined within 3.7.2 of metal cross-sectional area as deposited on the flat surface) is cause for rejection.



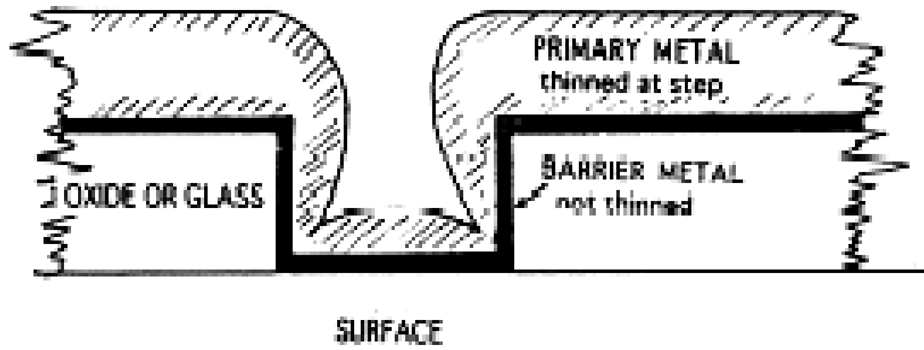


Figure 2018.24 20% metallization coverage (barrier metal inclusive)

APPENDIX A

Metal integrity alternate to SEM inspection

10. PURPOSE. Metal integrity is achieved through a system of designing and building in quality and reliability. It is not practical or cost effective to rely solely on end-of-line testing to ensure metal integrity. This procedure provides a system for designing, building, and monitoring a metal system that withstands the operating conditions of the device for the specified lifetime.

20. SCOPE

20.1 Utilization of this method provides an alternate to the requirements defined in TM2018. This procedure must be used in conjunction with the requirements of alternate 2 of TM5004, paragraph 3.3.1 as it applies to metallization.

20.2 This procedure describes a method by which metal integrity is assured through a combination of design rules and techniques, process development, manufacturing controls and end-of-line screening and reliability testing.

20.2.1 Design controls.

a. Reliability rules.

b. Layout rules.

c. Rules checking.

d. Process development.

20.2.2 Manufacturing controls. Statistical control of the manufacturing process and equipment defect and foreign material control.

20.2.3 Reliability testing. Accelerated tests.

30. DEFINITIONS

Lifetime. The mean time to failure of a technology at operating conditions defined to be normal. The mean time to failure is measured on a large sample of devices stressed at temperatures and current densities well above the normal operating conditions and extrapolated to normal operating temperature and current density.

Current density. The maximum allowable current density calculated as described in appendix A of MIL-PRF-38535.

Specification limits. Minimum or maximum boundaries for the value of a measured parameter. Material whose measured values are beyond these boundaries must be reviewed and dispositioned.

Worst case operating conditions. Conditions of current and temperature at which a device would normally operate, that would result in the greatest likelihood of failure.

40. REQUIREMENTS

40.1 Design controls. Design includes device design and process development. Device design includes all steps and supporting systems needed to translate a functional description for a device into a pattern generating data base. Process development includes selection of materials, tooling, and process conditions that may significantly affect metal integrity. The design process is a major consideration in establishing metal integrity.

40.1.1 A manufacturer's design system must include controlled, documented rules based on the manufacturer's processing capabilities. These rules shall specify feature size and spacing requirements, taking into account size changes that occur during processing. Manufacturers shall be able to justify their rules based on expected process variations. In addition, documented reliability rules shall exist which establish the electrical characteristics for each technology, taking into account processing materials, tolerances and limitations. The manufacturer shall have a system for checking designs for rule violations, and a system for correcting violations. Design rules shall consider the maximum current density (calculated as described in appendix A of MIL-PRF-38535) which shall be determined using worst case operating conditions and taking into consideration current crowding at contacts and vias. The manufacturer shall ensure that worst case processing conditions (such as alignment, metal thickness, line width, and contact/via size) do not result in violation of current density. Current density for a technology shall be at a level such that there is sufficient margin to ensure that failure will not result from electromigration in the specified lifetime of the device.

40.1.2 Process development. The manufacturer's design must take into consideration known levels of defects in the process. The process developed by the manufacturer must produce metallization that has the electrical and mechanical properties consistent with the design rules of 40.1.1, and reliability goals for the technology. Mechanical stress in the metal after final processing shall be understood. The manufacturer shall demonstrate, with results from appropriate designed experiments, that the desired electrical and mechanical properties have been achieved, and that the interaction of other process parameters on metal integrity parameters (minimum list in 40.2) is understood. The initial process specification limits shall be chosen such that metal integrity parameters are within the capability of the process. The manufacturer shall have a change control system in place such that new or changed processes are not put into production without the appropriate reliability evaluation.

40.2 Manufacturing controls. The manufacturer shall establish manufacturing controls in order to achieve uniformly good quality and reliability in their metal system, and to assure that the product is being manufactured according to the assumptions made during design. The manufacturer shall determine which parameters are critical to metal integrity and
* control those parameters in accordance with EIA-557-A. The manufacturer shall be able to demonstrate control of metal thicknesses, step coverage and cross-sectional areas, metal line width, contact and via sizes, contact and via resistance, and sheet resistance as a minimum, and show that they are being controlled to limits that are consistent with the way the metal system was designed. Specification limits shall be established for these parameters. In addition, defects that threaten metal integrity must be controlled in accordance with the alternate visual procedure (alternate 2) in appendix A of TM5004.

40.3 Reliability testing. While it is desirable to design in and build in reliability rather than to achieve reliability by screening finished product, there is valuable information to be gained from screening and reliability testing. Screening test such as burn-in not only eliminate the weaker parts in a population, but also provide information on failure mechanisms which can be used to improve design, materials, processes, or electrical test. Similarly, accelerated testing is used to speed up failure mechanisms likely to occur under normal operating conditions of a device. These failure mechanisms can then be analyzed to provide a basis for improvement. Accelerated test that a manufacturer may use to this end include but are not limited to electromigration testing, life testing, temperature-humidity-bias testing, and temperature cycling. Structures used in accelerated test must be typical of the technology represented. Failure mechanisms experienced during accelerated testing must be typical of those experienced during normal use of the device.

40.3.1 Reliability evaluating. The manufacturer must have in place a system for evaluating the reliability of the metal system. The system shall enable the manufacturer to determine the probability of failure in a given lifetime. The lifetime and failure rate data of the metal system associated with a given technology shall be made available to the customer. The manufacturer's systematically collected data must indicate that there is a high probability of meeting the specified lifetimes and/or failure rates.

50. DOCUMENTATION

NOTE: Certain information considered proprietary may only be available under non-disclosure agreement.

50.1 The manufacturer must have available for customer review controlled reliability rules, layout rules, and current density for each technology for which this procedure is used. In addition, the manufacturer must have available for review the method by which the above rules are checked and verified.

50.2 The manufacturer shall be able to demonstrate the manufacturing controls and system for disposition of out of control occurrences that are in place to control the processes determined critical to metal integrity.

50.3 The manufacturer must have available for customer review any testing performed to evaluate the reliability of the metal system.

50.4 The manufacturer shall specify the metal lifetime to the customer upon request.